Amendments to the Claims

Please amend claims 1 and 3 as follows:

1. (Currently Amended) A semiconductor memory, comprising:
data I/O buses;
a plurality of latch circuits connected in common to each of said data I/O buses;
a memory cell array including a plurality of bit line pairs, a plurality of bit switches connected between said plurality of latch circuits and said plurality of bit line pairs and divided into a plurality of groups, a plurality of column selection lines provided so as to correspond to said plurality of groups and each of which is connected to [[a]] the plurality of bit switches included in the corresponding group, and a plurality of sense amplifiers connected to said plurality of bit line pairs;
~~activating~~ said sense amplifiers adapted to activate when enabled by a ~~using an~~ sense amplifier enable signal;
a column decoder for driving said column selection lines; and
a control enable signal which controls the column decoder so as to drive two or more of said column selection lines in order during activation of said sense amplifiers.

2. (Original) The memory according to claim 1, wherein said memory cell array is divided into a plurality of blocks; said semiconductor memory further comprises a block selection signal for selecting said block; and
said sense amplifier enable signal activates said sense amplifiers in said selected block.

3. (Currently Amended) The memory according to claim 1, wherein said semiconductor memory operates in synchronization with an external clock; and

said control enable signal drives said two or more of said column selection lines in order ~~asynchronously~~ synchronously with the external clock.

4. (Currently Amended) A burst operation method for a semiconductor memory having data I/O buses, a plurality of latch circuits connected in common to each of said data I/O buses, and a memory cell array, in which said memory cell array includes a plurality of bit line pairs, a plurality of bit switches connected between said plurality of latch circuits and said plurality of bit line pairs and divided into a plurality of groups, a plurality of column selection lines provided so as to correspond to said plurality of groups and each of which is connected to [[a]] the plurality of bit switches included in the corresponding group, and a plurality of sense amplifiers connected to said plurality of bit line pairs, the burst operation method, comprising the steps of:
activating said sense amplifiers; and
driving two or more of said column selection lines in order during activation of said sense amplifiers.

5. (Original) The method according to claim 4, wherein said memory cell array is divided into a plurality of blocks; said burst operation method further comprises a step of selecting said block; and
the sense amplifiers in the selected block are selectively activated in said sense amplifier activating step.

6. (Original) The method according to claim 4, wherein said semiconductor memory operates in synchronization with an external clock; and
said two or more of the column selection lines are driven in order synchronously with the external clock in said column selection line driving step.